WHAT IS CLAIMED IS:

1. A memory system for data access and storage comprising:

a first array characterized by a first set of properties; and

a second array characterized by a second set of properties,

wherein the second set of properties differs from the first set of properties, and

wherein the first array and second array utilize a common addressing scheme and operate at different speeds and in conjunction with one another to output data.

2. The memory system of claim 1, wherein the first array operates at a first supply voltage and the second array operates at a second supply voltage.

3. The memory system of claim 2,

wherein the second supply voltage is higher than the first supply voltage, and

wherein the signal path from the second array to a memory controller is greater than the signal path from the first array to the memory controller, such that, after a request for data, which comprises a first data packet residing in the first array and a second data packet residing in the second array, is received by the first array and the second array, an output of the first data packet from the first array and an output of the second data packet output from the second array arrive at the controller at about the same time.

4. The memory system of claim 1, wherein the first array comprises a first wordline length and the second array comprises a second wordline length.

5. The memory system of claim 4,

wherein the wordline length of the second array is greater than wordline length of the first array, and

wherein the signal path from the second array to a memory controller is less the signal path from the first array to the controller, such that, after a request for data, which comprises a first data packet residing in the first array and a second data packet residing in the second array, is received by the first array and the second array, an output of the first data packet from the first array and an output of the second data packet output from the second array arrive at the controller at about the same time.

6. The memory system of claim 5, wherein the second array uses a higher supply voltage than the supply voltage used by the first array, such that, after a request for data, which comprises a first data packet residing in the first array and a second data packet residing in the second array, is received by the first array and the second array, an output of the first data packet from the first array and an output of the second data packet output from the second array arrive at the controller at about the same time.

7. The memory system of claim 1, wherein the first array comprises bitline sensing circuitry set at a system supply voltage, and the second array comprises bitline sensing circuitry operating at ground potential.

8. A method for storing data in and retrieving data from a semiconductor memory comprising:

linking a memory controller to a first memory array characterized by a first set of properties;

linking the memory controller to at least one other memory array characterized by a second set of properties, wherein the first and second set of properties are different;

storing a data packet, wherein a portion of the data packet is stored in the first array, and the remaining portion of the data packet is stored in the at least one other array; and

retrieving the data packet, wherein the data packet is retrieved in at least two portions, a first portion residing in the first array characterized by a first set of properties, and the remaining portion residing in the at least one other array characterized by a second set of properties.

9. The method of claim 8, wherein the data packet is retrieved after simultaneously signaling the first array and the at least one other array to output the data packet.

10. The method of claim 9, wherein the first portion of the data packet is output from the first array before the remaining portion of data is output from the at least one other array.

11. The method of claim 10, wherein the first array and the at least one other array are arranged such that the first portion of the data packet and the second portion of the data packet are received by the memory controller at about the same time.

12. The method of claim 8, wherein the portion of the data packet stored in the first array is divided into sub-portions, and the remaining portion of the data packet stored in the at least one other array is divided into sub-portions.

13. The method of claim 12, wherein the latency of the first array is less than the latency of the second array and the cycle time of the first array is greater than the cycle time of the at least one other array.

14. The method of claim 13, wherein the data packet is output in a plurality of sub-portions, the output sequence of the sub-portions being arranged in an ordered series, wherein the first array outputs the first sub-portion, and the second array outputs the second sub-portion.

15. A memory device, comprising:

a first memory array;

a second memory array;

a memory bus in communication with a memory controller,

wherein the first and second memory arrays utilize a same addressing scheme,

wherein the first and second memory arrays have at least one property different from one another, and

wherein for a given data retrieval event in the memory device, the first memory array outputs a first portion of data consistent with the data retrieval event and the second memory outputs a second portion of data consistent with the data retrieval event,

wherein the first portion of data and the second portion of data are received at the memory controller at about the same time.

16. The memory system of claim 15, wherein the first array operates at a first supply voltage and the second array operates at a second supply voltage.

17. The memory system of claim 15, wherein the first array comprises a first wordline length and the second array comprises a second wordline length.

18. The memory system of claim 15, wherein the first array comprises data sensing circuitry set at a system supply voltage, and the second array comprises data sensing circuitry operating at ground potential.

19. The memory system of claim 15, wherein the first array includes a plurality of sub-arrays.

20. The memory system of claim 19, wherein the second array includes a plurality of sub-arrays.